



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yi Ding
Assignee: Mosel Vitelic, Inc.
Title: Arrays of Nonvolatile Memory Cells Wherein
Each Cell Has Two Conductive Floating Gates
Application No.: 10/632,007 Filing Date: July 30, 2003
Examiner: Unknown Group Art Unit: Unassigned
Docket No.: M-15223 US

San Jose, California
September 17, 2003

Director of USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

No fee is believed to be required. If a fee is required for this Information Disclosure Statement, please charge the fee to Deposit Account No. 50-2257. This paper is being submitted in duplicate.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Director of USPTO, P.O. Box 1450, Alexandria, VA 22313-1450, on September 17, 2003.

Michael Shenker

Attorney for Applicant

9-17-03
Date of Signature

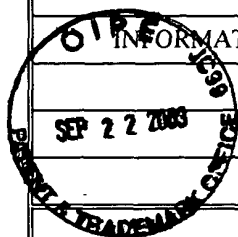
Respectfully submitted,

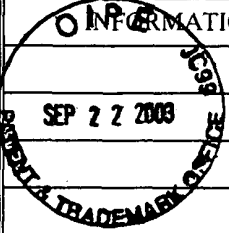
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U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				M-15223 US		10/632,007	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant			
(Use several sheets if necessary)				Yi Ding			
				Filing Date		Group	
				July 30, 2003		Unassigned	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
	AO						
	AP						
	AQ						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AR	United States Patent Application No. 10/440,466, entitled "Fabrication Of Conductive Gates For Nonvolatile Memories From Layers With Protruding Portions," Filed on May 16, 2003; Attorney Docket No.: M-12979 US.					
	AS	United States Patent Application No. 10/440,005, entitled "Fabrication of Dielectric On A Gate Surface To Insulate The Gate From Another Element Of An Integrated Circuit," Filed on May 16, 2003; Attorney Docket No.: M-15203 US.					
	AT	United States Patent Application No. 10/440,508, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories Having Select, Floating And Control Gates," Filed on May 16, 2003; Attorney Docket No.: M-15204 US.					
	AU	United States Patent Application No. 10/440,500, entitled "Integrated Circuits With Openings that Allow Electrical Contact To Conductive Features Having Self-Aligned Edges," Filed on May 16, 2003; Attorney Docket No.: M-15205 US.					
Examiner			Date Considered				
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>							



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		Yi Ding	
		Filing Date	Group
		July 30, 2003	Unassigned
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
	AV	United States Patent Application No. 10/393,212, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on March 19, 2003; Attorney Docket No.: M-12902 US.	
	AW	United States Patent Application No. 10/411,813, entitled "Nonvolatile Memories With A Floating Gate Having An Upward Protrusion," Filed on April 10, 2003; Attorney Docket No.: M-12903 US.	
	AX	United States Patent Application No. 10/393,202, entitled "Fabrication of Integrated Circuit Elements In Structures With Protruding Features," Filed on March 19, 2003; Attorney Docket No.: M-15151 US.	
	AY	United States Patent Application No. 10/631,941, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate," Filed on July 30, 2003; Attorney Docket No.: M-15171 US.	
	AZ	United States Patent Application No. 10/632,155, entitled "Nonvolatile Memory Cells With Buried Channel Transistors," Filed on July 30, 2003; Attorney Docket No.: M-15222 US.	
	BA	United States Patent Application No. 10/631,452, entitled "Fabrication Of Dielectric For A Nonvolatile Memory Cell Having Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15229 US.	
	BB	United States Patent Application No. 10/632,154, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15230 US.	
	BC	United States Patent Application No. 10/631,552, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on July 30, 2003; Attorney Docket No.: M-12902-1P US.	
	BD	United States Patent Application No. 10/632,186, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate And Having Upward Protrusions," Filed on July 30, 2003; Attorney Docket No.: M-15241 US.	
	BE		
	BF		
	BG		
	BH		
Examiner		Date Considered	
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